

Paper Title

Taro DENKI*, Jiro DENKI (Denki University)
Hanako DENSHI, Ichiro DENSHI (Denshi University)

Abstract

Most word limits are around 200 words.

Keywords: AVIC, ECT, Integrated circuit, Analog design, ..., (5–6 words).

1. Introduction

This template, using ieej-tec.cls for the PC, provides authors with most of the formatting specifications needed for preparing electronic versions of their papers. All standard paper components have been specified for three reasons: (1) ease of use when formatting individual papers, (2) automatic compliance to electronic requirements that facilitate the concurrent or later production of electronic products, and (3) conformity of style throughout a conference proceedings. Margins, column widths, line spacing, and type styles are built-in.

2. Section 2

2.1 Subsection

3. Conclusion

References

- (1) S.M. Park and H.-J. Yoo, “1.25-Gb/s regulated cascode CMOS transimpedance amplifier for gigabit ethernet applications,” *IEEE J. Solid-state Circuit* vol. 39, no. 1, pp. 112–121, Jan. 2004.



Fig. 1. AVIC logo.

Table 1. Device parameters.

M1 [μm]	W/L= 10/ 0.18
M2 [μm]	W/L= 60/ 0.18
C	0.25 pF